What is claimed is:

1. A method of creating a gate electrode, comprising the steps of:

providing a substrate, active surface regions having been defined in the surface of the substrate;

creating a layer of gate oxide over the surface of the substrate;

depositing a layer of gate material over the surface of the substrate;

creating a gate electrode structure;

creating a layer of liner oxide over the surface of said substrate, including sidewalls and the surface of said gate electrode;

depositing a layer of gate spacer material over the surface of said layer of liner oxide;

creating gate spacers over sidewalls of said gate electrode, thereby removing said layer of liner oxide from the surface of from sidewalls of said gate electrode where said layer of liner oxide is not covered with said gate spacers, expcsing first surfaces of said layer of liner oxide where said liner oxide is interposed between said layer of gate material and said gate spacers and where said liner oxide is furthest removed from the surface of said substrate, further exposing a second surface of

said layer of liner oxide where said layer of liner oxide overlies the surface of said substrate;

performing nitridation of said exposed first and second surfaces of said layer of liner oxide, creating a layer of silicon-oxy-nitride overlying the surface and exposed sidewalls of said gate electrode, further overlying said gate spacers and said exposed first and second surfaces of said layer of liner oxide;

removing said layer of silicon oxy-nitride; and

saliciding contact points to said gate electrode.

2. The method of claim 1, said layer of gate oxide being created to a thickness between about 50 and 150 Angstrom.

3. The method of claim 1, said layer of gate material comprising polysilicon.

4. The method of claim 1, said gate material being deposited to a thickness between about 3,000 and 7,000 Angstrom.

5. The method of claim 1, said gate spacer material comprising silicon nitride.

6. The method of claim 1, said gate spacer material being deposited to a thickness between about 2,000 and 3,000 Angstrom.

7. The method of claim 1, said layer of liner oxide being created to a thickness between about 100 and 500 Angstrom.

8. The method of claim 1, said nitridation being a N_2/H_2 plasma exposure.

9. The method of claim 1, said N_2/H_2 plasma exposure being performed at a temperature of about 250 degrees C.

10. The method of claim 1, said liner oxide comprising silicon oxide, said nitridation comprising a N_2/H_2 plasma treatment, thereby isotropically nitridizing the silicon oxide of said liner oxide to silicon oxy-nitride.

11. The method of claim 1, said saliciding contact points to said gate electrode being a cobalt base process of salicidation.

12. A method of reducing an etch rate of a layer of liner oxide for a gate electrode, comprising the steps of:

providing a substrate, active surface regions having been defined in the surface of the substrate;

creating a layer of gate oxide over the surface of the substrate;

depositing a layer of gate material over the surface of the substrate;

patterning and etching the layer of gate material and the layer of gate oxide, creating a gate electrode structure;

creating a layer of liner oxide over the surface of said substrate, including sidewalls and the surface of said gate electrode;

depositing a layer of gate spacer material over the surface of said layer of liner oxide;

etching said layer of gate spacer material, creating gate spacers over sidewalls of said gate electrode, thereby removing said layer of liner oxide from the surface of from sidewalls of said gate electrode where said layer of liner oxide is not covered with said gate spacers, exposing first surfaces of said layer of liner oxide where said liner oxide is interposed between said layer of gate material and said gate spacers and where said liner oxide is furthest removed from the surface of said substrate, further exposing a second surface of said layer of liner oxide where said layer of liner oxide overlies the surface of said substrate;

applying nitridation to said first and second surfaces of said layer of liner oxide, creating a layer of silicon oxy-

nitride overlying exposed surfaces of said gate electrode structure and said first and second surfaces of said layer of liner oxide;

removing said layer of silicon oxy-nitride; and

saliciding contact points to said gate electrode.

13. The method of claim 12, said applying nitridation to said first and second surfaces of said layer of liner oxide comprising a N_2/H_2 plasma exposure.

14. The method of claim 12, said applying nitridation to said first and second surfaces of said layer of liner oxide comprising a N_2/H_2 plasma exposure.

15. The method of claim 12, said layer of gate oxide being created to a thickness between about 50 and 150 Angstrom.

16. The method of claim 12, said layer of gate material comprising polysilicon.

17. The method of claim 12, said gate material being deposited to a thickness between about 3,000 and 7,000 Angstrom.

18. The method of claim 12, said gate spacer material comprising silicon nitride.

19. The method of claim 12, said gate spacer material being deposited to a thickness between about 2,000 and 3,000 Angstrom.

20. The method of claim 12, said layer of liner oxide being created to a thickness between about 100 and 500 Angstrom.

21. The method of claim 1, said saliciding contact points to said gate electrode being a cobalt base process of salicidation.

22. A method of reducing an etch rate of a layer of liner oxide for a gate electrode, comprising the steps of:

providing a substrate, active surface regions having been defined in the surface of the substrate;

creating a layer of gate oxide over the surface of the substrate;

depositing a layer of gate material over the surface of the substrate;

patterning and etching the layer of gate material and the layer of gate oxide, creating a gate electrode structure;

creating a layer of liner oxide over the surface of said substrate, including sidewalls and the surface of said gate electrode;

depositing a layer of gate spacer material over the surface of said layer of liner oxide;

etching said layer of gate spacer material, creating gate spacers over sidewalls of said gate electrode, thereby removing said layer of liner oxide from the surface of from sidewalls of said gate electrode where said layer of liner oxide is not covered with said gate spacers, exposing first surfaces of said layer of liner oxide where said liner oxide is interposed between said layer of gate material and said gate spacers and where said liner oxide is furthest removed from the surface of said substrate, further exposing a second surface of said layer of liner oxide where said layer of liner oxide overlies the surface of said substrate;

nitridizing the said first and second surfaces of said layer of liner oxide and second surfaces of said layer of liner oxide by exposing said first and second surfaces to a N_2/H_2 plasma at a temperature of about 250 degrees C., creating a layer of silicon oxy-nitride overlying exposed surfaces of said gate electrode structure and said first and second surfaces of said layer of liner oxide;

removing said layer of silicon oxy-nitride; and

saliciding contact points to said gate electrode.

23. The method of claim 22, said layer of gate oxide being created to a thickness between about 50 and 150 Angstrom.

24. The method of claim 22, said layer of gate material comprising polysilicon.

25. The method of claim 22, said gate material being deposited to a thickness between about 3,000 and 7,000 Angstrom.

26. The method of claim 22, said gate spacer material comprising silicon nitride.

27. The method of claim 22, said gate spacer material being deposited to a thickness between about 2,000 and 3,000 Angstrom.

28. The method of claim 22, said layer of liner oxide being created to a thickness between about 100 and 500 Angstrom.

29. The method of claim 22, said saliciding contact points to said gate electrode being a cobalt base process of salicidation.